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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/621,528	07/21/2000	Andreas Muhlberger	PHO 99-534	4855

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EXAMINER	
VAUGHAN, MICHAEL R	
ART UNIT	**PAPER NUMBER**
2131	

DATE MAILED: 06/29/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/621,528	MUHLBERGER ET AL.	
	Examiner	Art Unit	
	Michael R Vaughan	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Office Action

Claims 1-15 have been fully reconsidered and are pending.

Response to Arguments

Applicant's arguments filed 5-3-04 have been fully considered but they are not persuasive. Applicant alleges on page 3 of the immediate action that Reiner fails to disclose or suggest an additional memory access device, and the circuit pathway from the first storage location, through the first memory access device, the additional memory access device, the second memory access device, and finally to the second interface. The examiner respectfully disagrees for the following reasons.

The Examiner finds no language in the claimed invention that discloses the circuit pathway as argued on page 3. The language of independent claim 1 for example only says that the additional memory access means must cooperate with the second memory access means. The argument implies a linear or serial connection of the additional memory access means residing between the first memory access device and the second memory access device. Reiner discloses that an additional memory access (switching logic) means be implement by a ROM to actuate the plurality of switch (memory access means) (col. 3, lines 15-28). Therefore the Examiner finds there to be a circuit pathway to connect the additional memory access means with the second memory access. In response to applicant's argument that the references fail to show

certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., particular circuit pathway) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

For clarification, the Examiner has made the following interpretation of the equivalence between the claimed invention and Reiner's Fig. 1. The memory means is element 5. Both the first and second storage locations reside within the memory means 5. A first memory access means is element 3. A second memory access means is elements 7a-7c. An additional memory access means is element 4. A first interface is element 1, and the second interface is element 2.

With regard to the positioning of the claimed invention, Examiner finds limitations that a first memory access means is between first interface and memory means. This is present in Figure 1; elements 1->3->5 are electrical connected. A second memory access means arranged between the second interface and the memory means; elements 2->7a-7b->5 are electrically connected. Having element 3, first memory access means, in the circuit does not mean that 7a-7b are not still between 2 and 5.

For similar analysis, Examiner finds claim 7 and 13 anticipated by Reiner. For the reason mentioned above, the Examiner maintains the previous USC §102 and §103 rejections for the claimed invention.

Claim Rejections - 35 USC '102

Claims 1, 2, 6, 7, 8, 12, and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Reiner et al (USP 5,875,450).

As per claims 1 and 7, Reiner et al teach a data carrier (1) for the storage of data (column 2, line 6),

which data carrier (1) has a first interface (10) for communication with a first communication device (2) (column 2, line 15) and

which data carrier (1) has a second interface (25) for communication with a second communication device (3) (column 2, lines 16-17) and

which data carrier (1) includes an electrical circuit arrangement (12) (column 2, line 21),

which circuit arrangement (12) includes circuit parts (13, 14, 15) of the first interface (10) and circuit parts (27, 28, 29) of the second interface (25) (Figure 2, element 3) and

which circuit arrangement (12) has memory means (17) for the storage of data (Figure 1, element 5, which memory means (17) has a first storage location (22) and a second storage location (23) (column 2, line 23), and

which circuit arrangement (12) has a first memory access means (18), arranged between the first interface (10) and the memory means (17), for accessing the memory means (17) and which circuit arrangement (12) has a second memory access means (3

3), arranged between the second interface (25) and the memory means (17), for accessing the memory means (17) (Figure 1, element 7) and

which circuit arrangement (12) has access enabling means (21, 37, 39, 19) which enable the first storage location (22) to be accessed only by the first memory access means (18) (column 2, lines 34-35), characterized in that the data carrier (1) has additional memory access means (38) adapted to cooperate with the second memory access means (33) and adapted to access the first storage location (22) and designed to verify an access authorization for the access to the first storage location (22) (column 3, lines 17-21), and

in that after a positive result of the verification of the access authorization the second memory access means (33) can, in addition, access the first storage location (22) via the additional memory access means (38) and via the first memory access means (18) (column 2, lines 64-65).

As per claims 2 and 8, Reiner et al teach that the additional memory access means (38) are included in the first memory access means (18) (column 2, lines 38-41).

As per claims 6 and 12, Reiner et al teach the electrical circuit arrangement (12) of the data carrier (1) takes the form of an integrated circuit (column 2, line 21).

As per claim 13, Reiner et al teach a method (44) of accessing memory means (17) of a data carrier (1) having a first storage location (22) (Figure 1, element 5) and a

second storage location (23) (column 2, line 32), the method (44) comprising the steps defined hereinafter, namely

storing data in at least the first storage location (22) of the memory means (17) (column 2, lines 33-34),

enabling the first storage location (22) to be accessed only by the first memory access means (18), characterized in that access authorizations for access to the first storage location (22) are applied to additional memory access means (38) (column 2, lines 64-65), and

in that the applied access authorizations are verified with the aid of the additional memory access means (38) (column 3, lines 17-21), and in that after verification of the access authorizations and in the case of a positive result of the verification the first storage location (22) is accessed additionally by a second memory access means (33) via the additional memory access means (38) and via the first memory access means (18) (column 4, lines 45-53).

Claim Rejections - 35 USC ' 103

Claims 3, 5, 9, 11, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reiner et al.

As per claims 3, 9, and 14, Reiner et al teach that in order for a communication device to be able to access the protected memory, that an authorization process must first be performed and successfully passed (column 2, lines 64-65 and column 4, lines 45-53). Reiner teaches that a user can carry out this procedure. Reiner et al is silent in expressly disclosing the use of matching access codes to perform the authentication procedure. The use of access codes to grant a person to a secure resource is notoriously well known in the art. It would have been obvious to one of ordinary skill in the art to protect data stored in memory with an access code. Furthermore, it would be intuitively obvious to store a copy of the access code in a secure location such as the memory so that when authenticating a person the copy can be compared to the person's input.

In view of this, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Reiner et al to include an access code as a means to perform the authentication method of his system because access codes are a well known method in which to validate a person before granting him/her to a protected resource

As per claims 5, 11, and 15, Reiner et al teach that a first access condition must be verified in order to permit a user access to a protected memory (column 2, lines 38-45). Reiner also teaches that in order for a communication device to be able to access the protected memory, that an authorization process must first be performed and successfully passed (column 2, lines 64-65 and column 4, lines 45-53). Reiner teaches

a two-step validation process that must be passed in order to gain access to the protected memory of his system. Reiner et al is silent in expressly disclosing that a copy of the access condition is stored in the memory of the system and then compared to the access condition of the communicating user. One of ordinary of skill in the art would know that in order to check for an access condition, that the condition must be stored in memory. Furthermore, it would be advantageous to store the access condition in memory so it can be safe.

In view of this, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Reiner et al to store the access condition in memory and then check to see if the communicating user has positively met the access condition before granting the user access into the system's memory because it would add another level the security of the system in addition to the access code.

Claims 4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reiner et al in view of Schwartz et al (5,675,645).

As per claims 4 and 10, the examiner supplies the same rationale for the motivation to modify the teachings of Reiner et al to include the use of access codes as part of their authentication system. Reiner et al does not teach the use of triple DES to execute the authentication method. Schwartz et al teach the use of triple DES to help secure an authentication process in a system, which protects stored data in memory. It

would be advantageous to use encryption to guard against another user spying on the authentication process.

In view of this, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the teachings of Schwartz et al with the system of Reiner et al because it would allow the system to be more secure by not sending the access codes in plaintext.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael R Vaughan whose telephone number is 703-305-0354. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on 703-305-9648. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael R Vaughan
Examiner
Art Unit 2131

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